IN THE CLAIMS

Please cancel claims 24-26 as follows and amend the claims as follows.

1. (Currently amended) A field effect transistor, comprising:

a substrate;

a source and a drain;

an electric field terminal region in the substrate; and

a body above the electric field terminal region between the source and drain, wherein there is a barrier between the electric field terminal region and the body, wherein the electric field terminal region extends partially under the source and drain, and wherein all portions of the electric field terminal region have the same material type, that is either all portions are p-type or all portions are n-type.

2. (Original) The transistor of claim 1, wherein the barrier is an insulator layer between the body and the electric field terminal region.

3. (Original) The transistor of claim 1, wherein the body is undoped.

4. (Currently amended) A field effect transistor, comprising:

an insulator layer;

a body above the insulator layer between a source and a drain;

a substrate below the insulator layer;

a gate above the body and between the source and drain, the gate having a length; and

an electric field terminal region in the substrate, wherein the electric field terminal region extends partially under the source and drain, and wherein all portions of the electric field terminal region have the same material type, that is either all portions are p-type or all portions are n-type.

5. (Original) The transistor of claim 4, wherein the body is undoped.

6. (Original) The transistor of claim 4, wherein the body is lightly doped.

7. (Original) The transistor of claim 4, wherein a channel is formed in the body between the source and drain when certain voltages are applied to the source, gate, and drain, and the channel is undoped.

8. (Original) The transistor of claim 4, wherein a threshold voltage is set by a distance between the insulator layer and a gate insulator.

9. (Original) The transistor of claim 4, wherein the body floats.

10. (Original) The transistor of claim 4, wherein the body is biased.

11. (Original) The transistor of claim 4, wherein the electric field terminal region floats.

12. (Original) The transistor of claim 4, wherein the electric field terminal region is biased.

13. (Original) The transistor of claim 4, wherein the substrate floats.

14. (Original) The transistor of claim 4, wherein the substrate is biased.

15. (Original) The transistor of claim 4, wherein the electric field terminal region extends beneath essentially the entire length of the gate.

16. (Original) The transistor of claim 4, wherein the electric field terminal region extends beneath only a portion of the gate and another electric field terminal region extends beneath another portion of the gate.

17. (Original) The transistor of claim 4, wherein the transistor is a pMOSFET.

18. (Original) The transistor of claim 4, wherein the transistor is an nMOSFET.

19. (Canceled)

20. (Currently amended) A die comprising:

first and second field effect transistors each including:

(a) a substrate;

(b) ~~an electric field terminal region in the substrate.~~ a source, a drain, and a gate;

(c) ~~a source and a drain~~ a first electric field terminal region extending partially beneath the source and partially beneath the gate, and a second electrical field terminal region extending partially beneath the drain and partially beneath the gate; and

(d) a body above the electric field terminal ~~region~~ regions between the source and drain~~, wherein the electric field terminal region extends partially under the source and drain~~.

21. (Original) The die of claim 20, further comprising an insulator layer between the substrate and body.

22. (Original) The die of claim 20, wherein the insulator layer is shared by the first and second field effect transistor.

23. (Original) The die of claim 20, wherein the body is shared by the first and second field effect transistors.

24. - 26. (Canceled)